**CECS Interdisciplinary Design Program**

**Project Proposal Form**

Sponsoring Organization: *Northrop Grumman*

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Project Contact: *Marlon Fuentes*

Position: *Systems Engineering Manager*

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Project Title: *Digital ASIC Tapeout*

1. Background of Company/Organization: Provide a brief overview of the company and/or organization and the specific project location here. *Northrop Grumman solves the toughest problems in space, aeronautics, defense, and cyberspace to meet the ever-evolving needs of our customers worldwide. Our 95,000 employees are Defining Possible every day using science, technology and engineering to create and deliver advanced systems, products and services.*
2. Statement and Scope of the Problem(s): Provide the problem statement. Please be as specific as possible to help us understand the scope of the problem, and thus the scope of the project, specifically the design content.
   1. *Context: Northrop Grumman sees persistent challenges with ASIC talent in the workforce. We want to build a pipeline of undergraduate talent that is proficient in the full-flow digital ASIC design process.*
   2. *Senior Design Focus: The Senior capstone team is challenged with planning, executing, documenting, and providing designs for an ASIC.*
3. Overall Project Goal(s): Describe the overall goals of the project.
   1. *Context: Build a pipeline of undergraduate talent that is proficient in the full-flow digital ASIC design process.*
   2. *Senior Design Focus: Successfully tapeout an Application Specific Integrated Circuit (ASIC) implementing the RISC-V instruction set using existing electronic design automation (EDA) tools and relevant design technology libraries (~45nm or less). Goals of the team should include gaining relevant knowledge surrounding the ASIC design flow, Cadence tooling, troubleshooting, and the development of project documentation.*
4. Project Objectives: Describe the project objectives that will help achieve the goals of the project. Please be as specific as possible.
5. *Phase 1*
   * 1. *Design an ASIC implementing the RISC-V RV32I base instruction set, except for memory ordering and environment/system calls.*
     2. *Perform functional and/or formal verification of the design to confirm functionality of the design. Use the Universal Verification Methodology (UVM) standardized methodology. Target a minimum of 85% code coverage.*
     3. *Synthesize the hardware description language into a netlist for physical layout. Target the 45nm FreePDK45 technology using the Nangate open cell library.*
     4. *The design should be capable of processing 100 million instructions per second (100 MIPS) within the operating range of 0.95-1.25V and 0-125°C and consume a maximum of 1W. Additionally, the design should incorporate an L1 cache of at least 16MB.*
     5. *Test the performance and system-level functionality of the design by creating and executing test cases in RV32I assembly.*
6. *Phase 2*
   * 1. *Finalize functional and/or formal verification of the design, adhering to the target code coverage.*
     2. *Use electronic design tools to perform physical design and create a layout of the design.*
     3. *Conduct static timing analysis (STA), IR drop, and electromigration analysis to ensure physical performance requirements are met. Target a maximum IR drop of 5% with no timing failures and maximum current density within limits.*
     4. *Use physical design techniques such as design rule checking (DRC) to establish design manufacturability and layout versus schematic (LVS) to ensure correctness of the physical design.*
7. *Stretch goals*
   1. *Insert design for test (DFT) structures to validate functionality of a manufactured IC.*
   2. *Perform gate-level simulation to verify the design with real clock delays.*
   3. *Use logic equivalence checking to validate the functional equivalence between different stages of the development process.*
8. Expected Project Deliverables: Describe the expected project deliverables. Please be as specific as possible.
   1. *Mock tapeout a chip in at maximum 45 nm technology using* [*Cadence*](https://www.cadence.com/en_US/home.html) *digital design, verification, and signoff tools.* 
      1. *Deliverables for Phase 1 should include RTL design, initial verification metrics, and the synthesized netlist.*
      2. *Deliverables for Phase 2 should include finalized verification metrics, a GDSII file, a clean timing report, and IR drop and electromigration within specifications.*
   2. *Leverage the Cadence resources including training resources and Rapid Adoption Kits (RAKs) to acclimate students to the ASIC design flow and accelerate project completion.*
9. Core Competencies and Experience of Team: Please list required competencies, experience and/or knowledge needed by the project team members that will facilitate successful project execution.

*Students should have fundamental knowledge of:*

* 1. *Microelectronics and integrated circuits*
  2. *Synchronous digital design and Boolean logic*
  3. *Hardware description languages*
  4. *Computer architecture*
  5. *Automated design tools*

1. Other Special Considerations and Project Requirements: Please provide any special circumstances, constraints, resources, and requirements needed for the project.
   1. *US Citizenship (no Green Card)*
   2. *Willingness to explore job opportunities as an ASIC designer in the defense industrial base*
2. Project Liaison(s): If different than who is listed above, please provide the contact information and title/position for the project liaison(s).
   1. Lingerfelt, Aaron [Aaron.Lingerfelt@ngc.com](mailto:Aaron.Lingerfelt@ngc.com)
   2. Reategui, Alberto [Alberto.Reategui@ngc.com](mailto:Alberto.Reategui@ngc.com)

**UCF iDesign Project 2024-2025 Resources List**

Phase 1 (Fall Semester)

1. Fundamentals

* Semiconductors 101 (Cadence)
* Digital IC Fundamentals (Cadence)
* RTL-to-GDSII (Cadence)

1. Function/Formal Verification

* SystemVerilog for Design and Verification (Cadence)
* SystemVerilog Accelerated Verification with UVM (Cadence)
* [Setting Up a Basic Testbench Using UVM](https://www.chipverify.com/tutorials/uvm)
* [Video showing the UVM Testbench Design Process](https://www.youtube.com/watch?v=2026Ei1wGTU&pp=ygURYWx1IHV2bSB0ZXN0YmVuY2g%3D)
* [Code Coverage](https://www.chipverify.com/verification/code-coverage)
* [HDLBits -- Verilog](https://hdlbits.01xz.net/wiki/Main_Page)

1. Hardware Synthesis and Static Timing Analysis

* Genus Synthesis Solution (Cadence)
* Basic Static Timing Analysis (Cadence)

Phase 2 (Spring Semester)

1. Physical Design and Design Layout

* Innovus Block Implementation (Cadence)

1. IR Drop and Electromigration

* Voltus Power Grid Analysis and Signoff (Cadence)

1. Design Rule Checking and Layout Versus Schematic

* Pegasus Verification System (Cadence)

**Digital ASIC Tapeout Fall Schedule**

* Kickoff Meeting
  + Date: September 5, 2024
  + Objectives
    - Introduce the student team
    - Introduce the NGC team
    - Go over project goals and objectives
    - Any additional topics as necessary

Deadlines

* Initial Design
  + Deadline: September 27, 2024
  + Objectives
    - Give a list of instructions you plan to implement, as well as their function
    - Create a block diagram showing the hardware you plan to implement
    - Any additional early project objectives as necessary
* Midterm
  + Deadline: November 1, 2024
  + Objectives
    - 50% completion milestone, complete a minimum of 50% design work and begin initial verification work
    - Complete all Cadence courses listed under “Fundamentals” as well as at least one additional course under either “Functional/Formal Verification” or “Hardware Synthesis and Static Timing Analysis”
      * Completing additional courses and/or any Rapid Adoption Kits (RAKs) would be a bonus
* End of Semester
  + Deadline: November 26, 2024
  + Objectives
    - Complete all phase 1 deliverables, including design RTL, initial verification reports, and a synthesized netlist

**Progress Review**

* Project Progress Meetings
  + Scheduled as necessary or every two weeks
  + Objectives
    - Review current project progress
    - Address student questions to the NGC team
    - Any additional topics as necessary
* End of Semester Meeting
  + Date: TBD
  + Objectives
    - Go over semester accomplishments, next steps for spring semester